Temporary position or post-doc
micro-electronics engineer/physicist

The IRFU microelectronics group has 30 years of experience in analog and mixed-circuit low-noise integrated circuit design for particle detection. It consists of a dozen engineer-researchers.

The main areas of expertise are multichannel front-end ASICs, fast analog memories, monolithic active pixels, ultra-cryogenic microelectronics and time measurement at the picosecond level. More than 400,000 detection channels designed by the group equip different instruments, worldwide, on Earth or in space.

The present project includes a consortium of several research laboratories led by the laboratory Leprince Ringuet (LLR) at Ecole Polytechique in Palaiseau.

The goal is to design a new type of beam monitor capable of detecting and continuously locating a beam of particles coming from an accelerator. The monitor includes the detector and its multi-channel readout electronics. This development is motivated by the needs of proton therapy, but its scope goes beyond medical applications.

The project has 4 phases: the study of the signal generation, the radiation resistance, the design of the integrated low noise readout electronics (ASIC), and assembly and tests of the complete system.

IRFU is responsible for the design of the integrated readout circuit.

The main task will be to design and simulate a complete readout circuit of the particle detector designed by LLR. This circuit will feature at least 8 identical read channels. Each channel will have to measure very precisely the current delivered by the detector, on a dynamic range of 6 decades.

The choice of manufacturing technology (foundry) remains open. Different architectures can be explored by taking into account the specifications coming from the detector parameters (capacitance, current dynamics) and the application (max processing time, counting rate ...). Depending on the manufacturing technology chosen, the candidate will be able to benefit from existing microelectronic blocks that have been tested.

The second task is to prepare the circuit tests: design and implementation of the board and the test bench.

The third and final task will be to participate in the chip tests.

Candidate Profile
The candidate must have a degree in engineering and / or Ph D in microelectronics. He (she) must have designed and tested at least one analog or mixed ASIC.

He or she will of course have to master perfectly the Cadence CAD tool and also master the tools of CAD PCB to be able to design or participate in the design of the test systems. The

candidate must be able to work in a team, and in particular to communicate with the detector and electronics teams downstream, but also be autonomous. His adaptability will allow him/her to be operational very quickly.

You may find the same information in French and submit your application at the following link : https://www.emploi.cea.fr/offre-de-emploi/emploi-drf-irfu-dedip-stream-cdd-ingenieur-en-micro-electronique-h-f_5577.aspx

Do not hesitate to contact Olivier Gevin (olivier.gevin@cea.fr) for discussion and further information.